SSC8127GS6

P-Channel Enhancement Mode MOSFET

➢ Features

VDS	VGS	RDSON Typ.	ID
-20V	±12V	135mR@-4V5	-1.8A
		175mR@-2V5	
		260mR@-1V8	

➢ Description

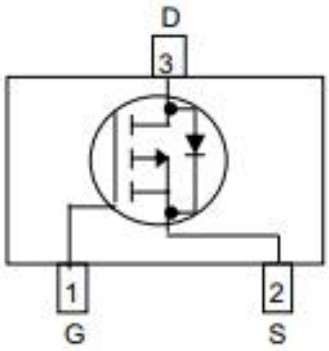
This device is produced with high cell density DMOS trench technology, which is especially used to minimize on-state resistance. This device particularly suits low voltage applications such as portable equipment, power management and other battery powered circuits, and low in-line power dissipation are needed in a very small outline surface mount package.

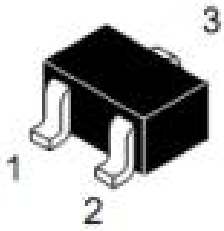
➢ Applications

- Load Switch
- Portable Devices
- DCDC conversion

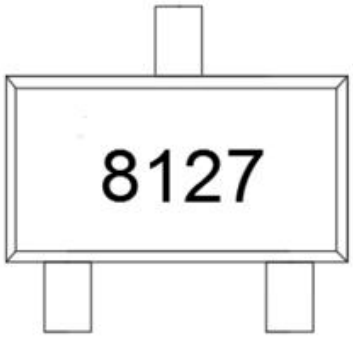
➢ Pin configuration

Top view





SOT23



Marking

➢ Ordering Information

Device	Package	Shipping
SSC8127GS6	SOT23	3000/Reel

➢ Absolute Maximum Ratings(T_A=25℃ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	-20	V
V_{GSS}	Gate-to-Source Voltage	±12	V
I_D	Continuous Drain Current [a]	-1.8	A
I_{DM}	Pulsed Drain Current [b]	-6	A
P_D	Power Dissipation [c]	0.65	W
P_{DSM}	Power Dissipation [a]	0.4	W
T_J	Operation junction temperature	-55 to 150	℃
T_{STG}	Storage temperature range	-55 to 150	℃

➢ Thermal Resistance Ratings(T_A=25℃ unless otherwise noted)

Symbol	Parameter	Typical	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance [a]		240	℃/W
$R_{\theta JC}$	Junction-to-Case Thermal Resistance		147	

Note:

a. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in^2 FR-4 board with 2oz.copper,in a still air environment with T_A=25℃.The value in any given application depends on the user is specific board design. The current rating is based on the t≤ 10s thermal resistance rating.

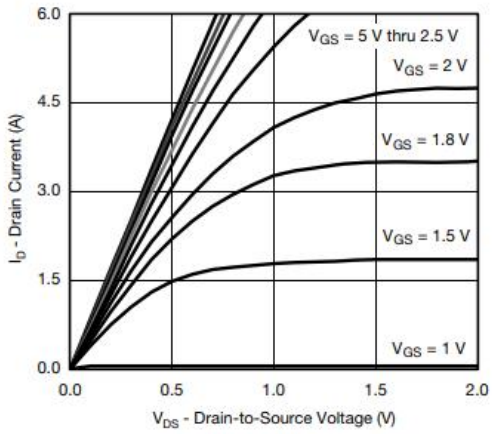
b. Repetitive rating, pulse width limited by junction temperature.

c. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

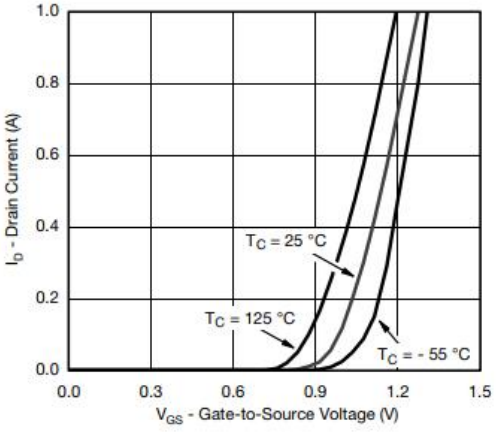
➢ **Electronics Characteristics**(T_A=25℃ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	VGS=0V,ID=-250uA	-20			V
$V_{GS\ (th)}$	Gate Threshold Voltage	VDS=VGS,ID=-250uA	-0.4	-0.7	-1	V
$R_{DS(on)}$	Drain-Source On-Resistance	VGS=-4.5V,ID=-2A		135	170	mR
		VGS=-2.5V,ID=-1A		175	220	
		VGS=-1.8V,ID=-0.5A		260	450	
I_{DSS}	Zero Gate Voltage Drain Current	VDS=-20V,VGS=0V			-1	uA
I_{GSS}	Gate-Source leak current	VGS=±12V,VDS=0V			±100	nA
G_{FS}	Transconductance	VDS=-5V,ID=-1A		3		S
V_{SD}	Forward Voltage	VGS=0V,IS=-1A			-1.3	V
Ciss	Input Capacitance	VDS=-10V, VGS=0V, f=1MHZ		315		pF
Coss	Output Capacitance			19		
Crss	Reverse Transfer Capacitance			15		
Qg	Total Gate Charge	VGS=-4.5V, VDS=10V, ID=1A		4.3		nC
Qgs	Gate Source Charge			1.8		
Qgd	Gate Drain Charge			1.5		
$T_{D(ON)}$	Turn-on delay time	VGS=4.5V, VDS=10V, RG=6R, RL=20R		5		ns
$T_{D(OFF)}$	Turn-off delay time			29		

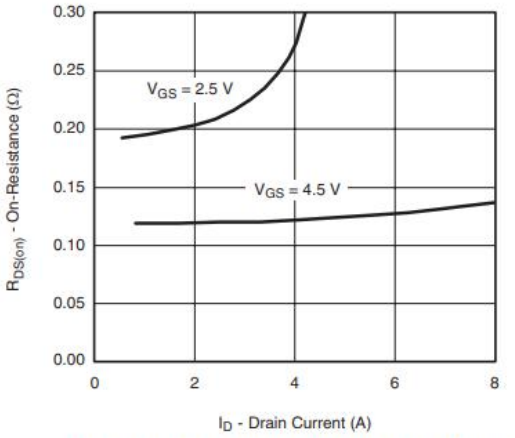
➢ Typical Characteristics(T_A=25℃ unless otherwise noted)



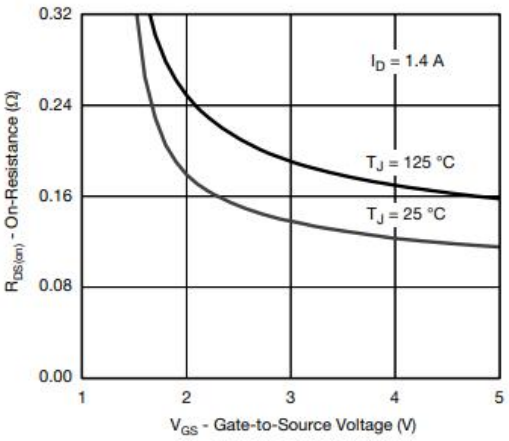
Output Characteristics



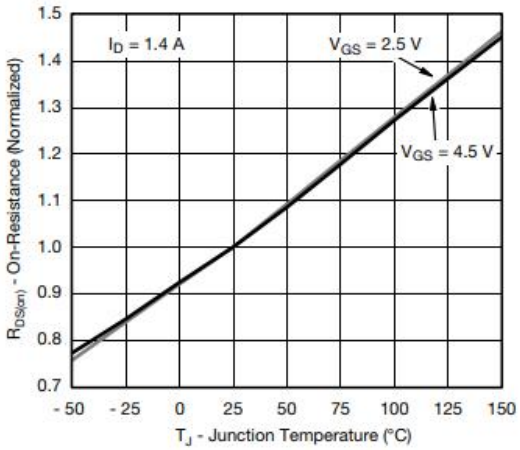
Transfer Characteristics



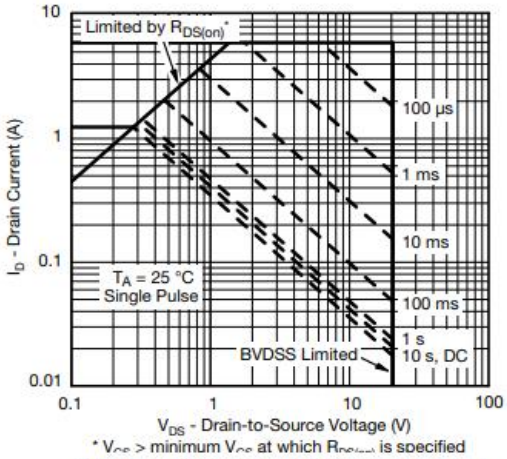
On-Resistance vs. Drain Current and Gate Voltage



On-Resistance vs. Gate-to-Source Voltage

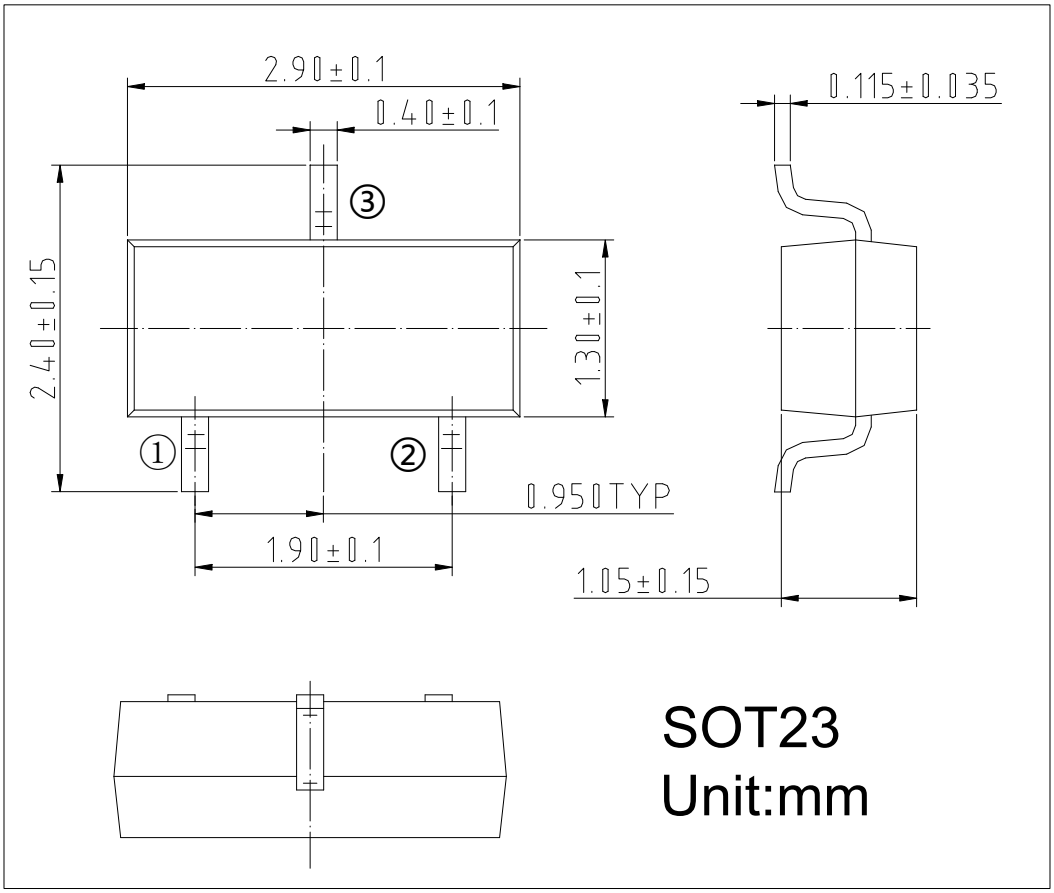


On-Resistance vs. Junction Temperature

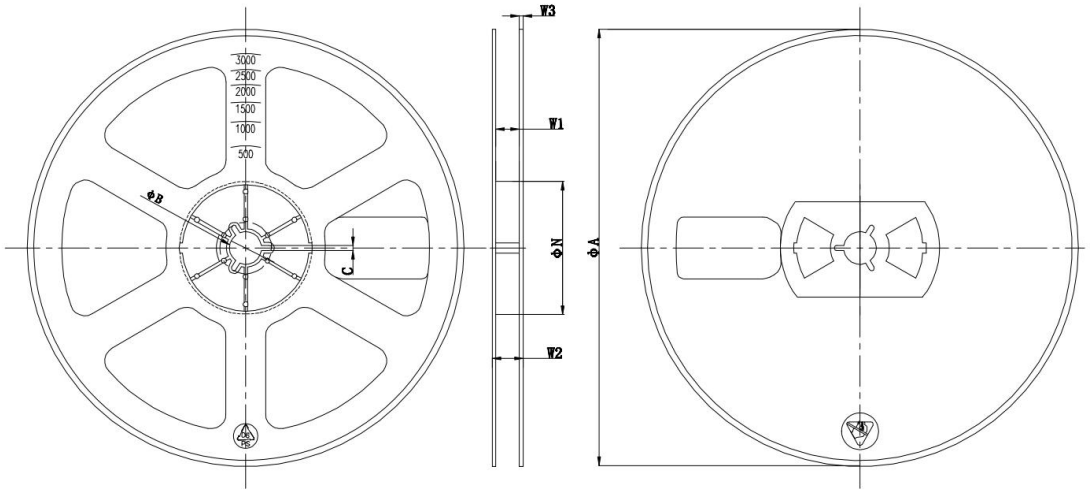


Safe Operating Area, Junction-to-Ambient

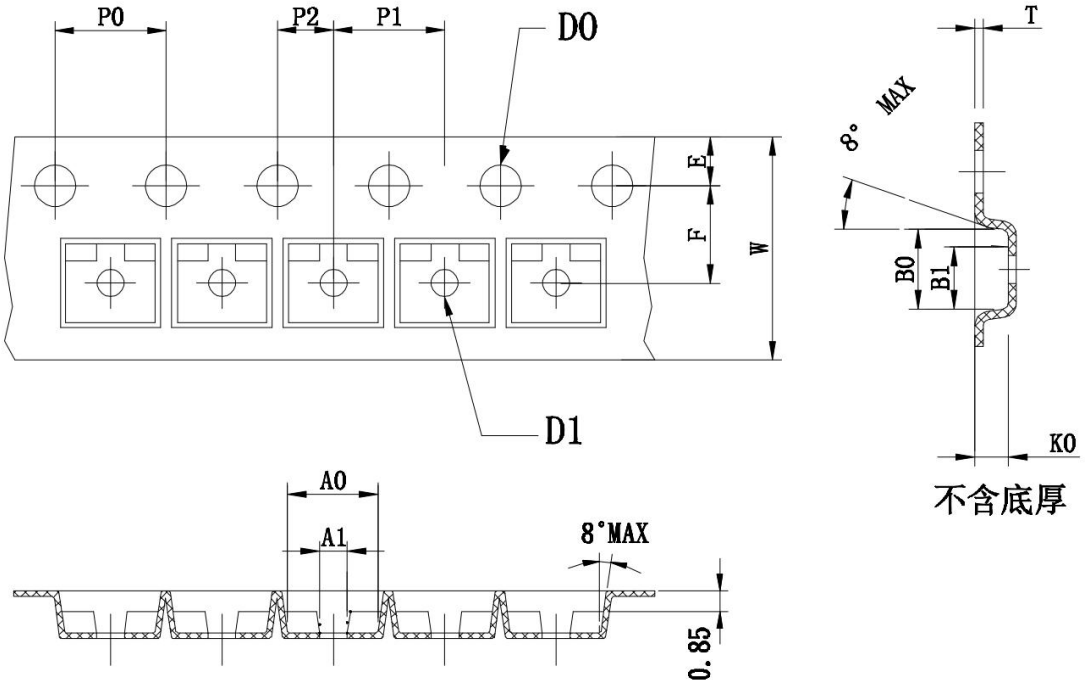
➢ Package Information



➢ Tape and Reel



ΦA	ΦN	ΦB	C	W1	W2	W3
178±2	54±2	13.2±0.3/0.2	2.2±0.3	9.5±1	13max	1.4±0.4



Symbol	A0	A1	B0	B1	K0	D0	D1	P0
Spec	3.15±0.10	1.15±0.10	2.80±0.10	2.15±0.10	1.30±0.10	1.55±0.10	1.10±0.10	4.00±0.10
Symbol	P1	W	E	P2	T	10*P0	F	
Spec	4.00±0.10	8.00±0.10	1.75±0.10	2.00±0.10	0.21±0.02	40.00±0.10	3.50±0.10	

➢ History Version

V1.0	Product datasheet release	2021-01-04
V2.0	Cancel Ron@VGS=-1.8V test item	2021-03-30
V3.0	V_{GS} Max changed from "0.9" to "1";R_{DSON} 1.8V Typ changed from "240" to "260"； R_{DSON} 1.8V Max changed from "300" to "450".	2022-08-30

DISCLAIMER

AFSEMI RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. AFSEMI DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICIENCE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

THE GRAPHS PROVIDED IN THIS DOCUMENT ARE STATISTICAL SUMMARIES BASED ON A LIMITED NUMBER OF SAMPLES AND ARE PROVIDED FOR INFORMATIONAL PURPOSE ONLY. THE PERFORMANCE CHARACTERISTICS LISTED IN THEM ARE NOT TESTED OR GUARANTEED. IN SOME GRAPHS, THE DATA PRESENTED MAY BE OUTSIDE THE SPECIFIED OPERATING RANGE (E.G. OUTSIDE SPECIFIED POWER SUPPLY RANGE) AND THEREFORE OUTSIDE THE WARRANTED RANGE.